

**SHAID SMARAK COLLEGE**

Kirtipur, Kathmandu, Nepal

*Lab Sheet 8 of Digital Logics*

**Submitted by :-**

1st semester

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**Submitted to :-**

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**OBJECTIVE:**  TO CONSTUCT THE MOD-1O ASYNCHRONOUS COUNTER

**EQUIPMENT NEEDED**:

Breadboard

9v battery

Led bulbs

Jumper wires

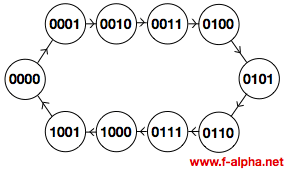
5v registers

Toggles switches

IC 7400 (NAND GATE)

**MOD-10 COUNTER OR DECADE COUNTER OR BCD COUNTER**

As we know mod- 10 counter is the asynchronous counters, So here clock pulse is not same for all clock. In Mod-10 counter, it consists 10 no. of clock pulse. We know N=2^n, when we put n=4, we get 2^n=2^4=16, which is greater than 10(16>10). Thus, we used 4 flip flops to design the mod-10 counter. It counts from 0000 to 1001 i.e. in decimal from 0 to 9. It has 10 no. of states.



**STATE DIAGRAM OF MOD-10 COUNTER (DECADE COUNTER)**

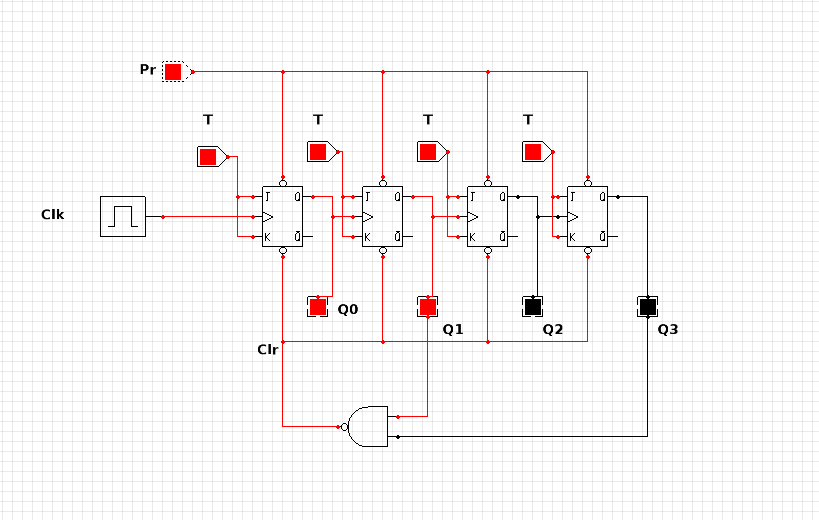
The different clock pulse is passed to the clock input of all the flip flops as the asynchronous counters. Here, we used overriding or direct input as clear and presets. The output is 1 when the preset set to 0.

The output is 1 when the clear set to 0. Both the preset and clear always work in value 0, because they are active low signals.

i.e. Pr=0 , Q=1 Pr=1 ,

Clr=0 , Q=O Clr=1 , NORMAL OPERATION

These two values is always fixed and independent with the input T and the clock pulse.



**Circuit diagram of MOD—10 counter**

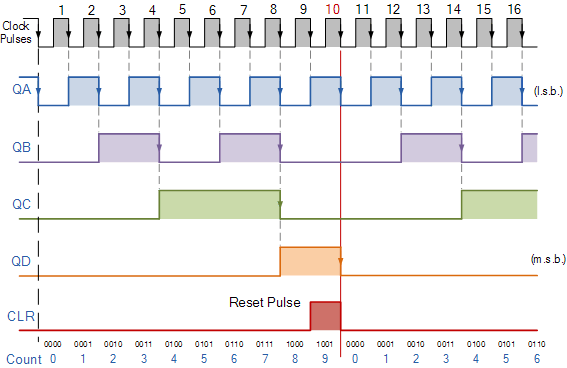
Here, Q0 is consider as LSB(Least Significant Bit)and Q3 is as MSB(Most Significant Bit). All T inputs are equal to 1. The small circle in the clock pulse input indicates that the flipflops complements during a negative going transition or when the output to which it is connected goes from 1 to 0.

As we know the characteristic table of T flipflops.

|  |  |
| --- | --- |
| T | Qn+1 |
| O | Qn |
| 1 | Q’n |

When the value of T is equal to 1 the next state will be the complement state i.e. toggling mode of T flipflop.

Now, we draw the timing diagram of mod-10 asynchronous counter.

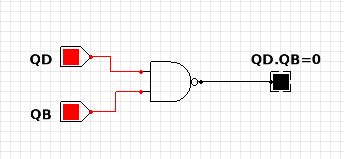


The state of the output QA changes when the negative clock edge passes to the flip flop. Initially, all the flipflops are set to 0. These flipflops changes their state when the passed clock goes from 1 to 0.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| No. of clock pulse | Q3 | Q2 | Q1 | Q0 | Clear (Clr) |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 1 |
| 5 | 0 | 1 | 0 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 1 |
| 7 | 0 | 1 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 | 1 |
| 10 | 1 | 0 | 1 | 0 | 0 |
| 11 | 1 | 0 | 1 | 1 | \* |
| 12 | 1 | 1 | 0 | 0 | \* |
| 13 | 1 | 1 | 0 | 1 | \* |
| 14 | 1 | 1 | 1 | 0 | \* |
| 15 | 1 | 1 | 1 | 1 | \* |

**State table of MOD-10 asynchronous counter**

When it count up to 9 (1001) and in next state 10 (1010) the output of the QB and QD is equal to 1 but we need zero in place of these outputs. So here we use NAND gate for this operation



Thus, the zero inputs is passes through the clears inputs of all the flipflops. As we already discuss when the value 0 is passes through clear, the output of flipflops will equal to zero because clear is active low signals.

Hence, we get 0000 after 1001 in MOD-10 counter.